REMARKS:

Claims 1-5 and 54 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. 4,142,150 (Morrow). In response, Applicants respectfully contend that claims 1-5 and 54 are patentable over Morrow for the following reasons.

Claim 1 recites a sensing apparatus including at least one sensor cell (configured to produce a sensor current indicative of a sensed value) and a readout circuit. The readout circuit has an input node (coupled to receive the sensor current), an output node, and output voltage generation circuitry (between the input node and output node) configured to generate an output voltage in response to the sensor current while clamping the input node at a potential that is at least substantially fixed.

Claim 54 recites a method for reading out a sensor cell, comprising the steps of asserting a sensor current (indicative of a sensed value) from the sensor cell to an input node of a readout circuit; and operating the readout circuit in response to the sensor current to generate an output voltage (indicative of the sensed value) while clamping the input node at a potential that is at least substantially fixed.

In Figs. 1 and 2, Morrow discloses a transistor (14 or 40), and a voltage generating circuit comprising elements 24, 26, 28, 30, and 22. The transistor's emitter current flows to an input node (the "negative input" of differential amplifier 22) of the voltage generating circuit. In response, the voltage generating circuit generates a voltage (at differential amplifier 22's output) indicative of the emitter current. Circuit 32 generates a current (an "emitter current reading") indicative of the voltage at the output of differential amplifier 22.

Even assuming for the sake of argument that Morrow's transistor 14 or 40 (or "device under test" 10 which includes transistor 14, or "device under test" 36 which includes transistor 40) corresponds to the recited sensor cell, and that the emitter current of transistor 14 or 40 is indicative of a sensed value (as is the recited sensor current), Morrow fails to teach or suggest that the input node of Morrow's voltage generating circuit is or should be clamped at a potential that is "at least substantially fixed" as claimed. Rather,

the input node of Morrow's voltage generating circuit is not clamped at a fixed (or substantially fixed) potential. The input node of Morrow's voltage generating circuit is specifically designed to have a variable potential that determines the potential at the output node (the output of amplifier 22) of Morrow's voltage generating circuit. The fact that a capacitor (capacitor 30) is coupled to the input node of Morrow's voltage generating circuit does not imply that such input node is or should be clamped at a fixed (or substantially fixed) potential.

Applicants respectfully contend that there is no basis determinable from Morrow or any other reference of record in support of the assertion in the Office Action that it "would have been obvious for one of ordinary skill in the art to modify Morrow by adding [sic] clamping the input node" at a fixed (or substantially fixed) potential. Instead, Morrow teaches away from clamping the input node of its voltage generating circuit, since clamping this input node at a fixed (or substantially fixed) potential would also clamp the output voltage of Morrow's voltage generating circuit at a fixed (or substantially fixed) potential, thereby preventing Morrow's voltage generating circuit from performing the function that Morrow teaches that it should perform.

Claims 2-5 are patentable over Morrow for the same reasons (set forth above) that claim 1 is patentable over Morrow.

An independent reason that claim 3 is patentable over Morrow is that Morrow fails to teach or suggest a readout circuit (an element distinct from the sensor cell recited in claim 3) that includes both a differential pair and a load transistor coupled to the differential pair, as recited in claim 3. Given the Examiner's contention that Morrow's differential amplifier 22 is a differential pair of a readout circuit as claimed and that Morrow's transistor 40 is an element (that produces a sensor current) of a sensor cell as claimed, neither transistor 38 nor transistor 40 of Morrow's Fig. 2 is a load transistor coupled to a differential pair as claimed. This is because transistor 38 is not coupled to differential amplifier 22, and transistor 40 is not an element of a readout circuit (in contrast with a sensor cell) as claimed.

If one contends for the sake of argument that Morrow's transistor 40 is a load transistor (as recited in claim 3) of a readout circuit (as recited in claim 1), then it cannot also

be contended reasonably that transistor 40 is a sensor cell (or sensor current-producing element of a sensor cell) as recited in claim 1, since the sensor cell and readout circuit of claim 1 are distinct elements. If Morrow's transistor 40 is not a sensor cell (or a sensor current-producing element of a sensor cell) as recited in claim 1, the Office Action articulates no basis for a contention that Morrow teaches or suggests the sensor cell of claim 3, and thus claim 3 is patentable over Morrow.

Claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Morrow in view of U.S. 4,816,768 (Champlin). In response, Applicants contend that claim 6 is patentable over the cited references for the following reasons.

Claim 6 is patentable over Morrow for the same reasons (set forth above) that claim 1 is patentable over Morrow.

Champlin, like Morrow, fails to teach or suggest clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node) as recited in claim 1. Thus, claim 1 (and claim 6) is patentable over Champlin considered alone.

There is no teaching or suggestion determinable from Champlin to modify Morrow's teaching by clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential. As explained above, clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential would also clamp the output voltage of Morrow's voltage generating circuit at a fixed (or substantially fixed) potential, thereby preventing the voltage generating circuit from performing the function that Morrow teaches that it should perform. Thus, claim 1 and claim 6 are patentable over the combined teaching of Morrow and Champlin, considered individually or in combination.

Claims 7, 55-56, and 58 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Morrow in view of U.S. 6,480,227 (Yoneyama). In response, Applicants contend that these claims are patentable over the cited references for the following reasons.

Claim 7 is patentable over Morrow for the same reasons (set forth above) that claim 1 is patentable over Morrow. Yoneyama, like Morrow, fails to teach or suggest clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node) as recited in claim 1. Thus, claim 1 (and thus claim 7) is patentable over Yoneyama considered alone.

Each of claims 55-56 and 58 is patentable over Morrow for the same reasons (set forth above) that claim 54 is patentable over Morrow. Yoneyama, like Morrow, fails to teach or suggest clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node) as recited in claim 54. Thus, claim 54 (and thus claims 55-56 and 58) are patentable over Yoneyama considered alone.

There is no teaching or suggestion determinable from Yoneyama to modify Morrow's teaching by clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential. As explained above, clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential would also clamp the output voltage of Morrow's voltage generating circuit at a fixed (or substantially fixed) potential, thereby preventing the voltage generating circuit from performing the function that Morrow teaches that it should perform. Thus, each of claims 1 and 54 (and each of claims 7, 55, 56, and 58) is patentable over the combined teaching of Morrow and Yoneyama, considered individually or in combination.

Claim 57 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Morrow in view of Yoneyama and Champlin. In response, Applicants contend that claim 57 is patentable over the cited references for the following reasons.

Claim 57 is patentable over each of Morrow and Yoneyama for the same reasons (set forth above) that claim 54 is patentable over Morrow and Yoneyama, considered individually or in combination. Champlin, like Morrow, fails to teach or suggest a method in which an input node of a readout circuit (configured to generate an output voltage in response to a sensor current at the input node) is clamped as recited in claim 54. There is no teaching or

suggestion determinable from either of Yoneyama or Champlin to modify Morrow's teaching by clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential. As explained above, clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential would also clamp the output voltage of Morrow's voltage generating circuit at a fixed (or substantially fixed) potential, thereby preventing the voltage generating circuit from performing the function that Morrow teaches that it should perform. Thus, claim 54 (and claim 57) is patentable over each of Morrow, Yoneyama, and Champlin considered individually or in combination.

Claims 59-61 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Morrow in view of Yoneyama and U.S. 5,059,916 (Johnson). In response, Applicants contend that these claims are patentable over the cited references for the following reasons.

Claim 57 is patentable over Morrow and Yoneyama, considered individually or in combination, for the same reasons (set forth above) that claim 54 is patentable over Morrow and Yoneyama. Johnson, like Morrow, fails to teach or suggest a method in which an input node of a readout circuit (configured to generate an output voltage in response to a sensor current at the input node) is clamped as recited in claim 54. There is no teaching or suggestion determinable from either of Yoneyama or Johnson to modify Morrow's teaching by clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential. As explained above, clamping the input node of Morrow's differential amplifier 22 at a fixed (or substantially fixed) potential would also clamp the output voltage of Morrow's voltage generating circuit at a fixed (or substantially fixed) potential, thereby preventing the voltage generating circuit from performing the function that Morrow teaches that it should perform. Thus, claim 54 (and each of claims 59-61) is patentable over the

teaching of Morrow, Yoneyama, and Johnson, considered individually or in combination.

Reconsideration and allowance of the rejected claims is respectfully requested.

Respectfully submitted,
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